//testbench

module tb\_bcd\_4digit\_counter;

reg clk;

reg rst;

wire [15:0] q;

wire [2:0] en;

bcd\_4digit\_counter uut ( .clk(clk), .rst(rst), .q(q), .en(en));

initial begin

$dumpfile("bcd\_4digit\_counter.vcd");

$dumpvars(1);

end

always begin

#5 clk = ~clk;

end

initial begin

clk = 0;

rst = 0;

#10 rst = 1;

#10 rst = 0;

#100 $finish;

end

endmodule

//design

module bcd\_4digit\_counter (

input wire clk,

input wire rst,

output reg [15:0] q,

output reg [2:0] en

);

reg [15:0] count;

always @(posedge clk or posedge rst) begin

if (rst) begin

count <= 16'b0000\_0000\_0000\_0000;

en <= 3'b000;

end else begin

if (count == 16'h9999) begin

count <= 16'b0000\_0000\_0000\_0000;

en <= 3'b000;

end else begin

count <= count + 1;

if (count[11:8] == 4'b1000) en[2] <= 1;

else en[2] <= 0;

if (count[7:4] == 4'b1000) en[1] <= 1;

else en[1] <= 0;

if (count[3:0] == 4'b1000) en[0] <= 1;

else en[0] <= 0;

end

end

end

always @\* begin

q[3:0] = count[3:0];

q[7:4] = count[7:4];

q[11:8] = count[11:8];

q[15:12] = count[15:12];

end

endmodule